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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,555	03/10/2004	Michael W. Morrow	P19083	7799

25694 7590 09/19/2006

INTEL CORPORATION
P.O. BOX 5326
SANTA CLARA, CA 95056-5326

EXAMINER	
NGUYEN, THAN VINH	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,555	MORROW, MICHAEL W.	
	Examiner	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,10,17-23,28-33,35,36,38-41 and 43-46* is/are rejected.

7)☒ Claim(s) *6-8,11-16,24-27,34,37 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1) Claims 1-46 are pending.

2) The IDS, filed 3/10/04.

Claim Rejections - 35 USC § 112

3) The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4) Claims 43-46 recites the limitation "the first processor" in line 4. There is insufficient antecedent basis for this limitation in the claim. Claims 44-46 are also rejected for incorporating this error.

Claim Rejections - 35 USC § 102

5) The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6) Claims 1-5, 9,10,17,19-23,28-33,39-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Marshall, Jr. et al (US 6,134,634) "Marshall".

As to claim 1,10,23,32,39:

7) Marshall teaches an apparatus/system and its associated method for: setting/storing a status corresponding to a block of data in response to a change in address mapping to indicate that

the block of data is pending write back (during context/process switching; set writeback bit P to indicate pending writeback; 2/58-3/7;5/3-15;9/28-51;11/40-56).

As to claim 2,28,33:

8) Marshall teaches further including changing the address mapping in response to switching from executing a first software process to executing a second software process, wherein the first software process uses a first address mapping and the second software process uses a second address mapping (context switching means the memory mapping of the processes are different; 2/58-3/7).

As to claim 3-5,40:

9) Marshall teaches preventing access to the data block until the writeback is completed (2/33-57).

As to claim 9:

10) Marshall teaches further comprising writing back the block of data from a first level of memory to a second level of the memory using either a demand driven write back scheme or a lazy write back scheme (delayed writeback; 2/50-57; 5/27-30).

As to claim 17:

11) Marshall teaches wherein the storage area is located in a cache memory (9/28-36).

As to claim 19,41:

12) Marshall teaches the apparatus is a processor (5/15). Applicant should note that renaming of the preamble from an "apparatus" to a "processor " does not give more patentable weight since no additional limitation is added to the body of the claim to signify the difference between an apparatus and a processor. The Examiner will treat the claimed invention of an apparatus and processor to be the same since both have the same limitations, as disclosed and claimed in the body of the claim.

As to claim 20,29:

13) Marshal teaches the processor includes logic to translate virtual addresses to physical addresses (translation; 6/60-67).

As to claim 21,30:

14) Marshall teaches the apparatus is a virtually addressed cache memory (6/60-67).

As to claim 22,31:

15) Marshall teaches the apparatus is a virtually addressed buffer (TLB; 6/60-67).

16) Claims 35,36,38 are rejected under 35 U.S.C. 102(e) as being anticipated by Middleton (US 6,564,301).

As to claim 35:

17) Middleton teaches a method, comprising: setting a dirty bit in a cache tag that is associated with a predetermined amount of cache data; and setting a write back bit in the cache tag (Fig. 3B, set D and WB bit 8/6-45).

As to claim 36:

18) Middleton teaches setting a valid bit in the cache tag and wherein the write back bit is set if the dirty bit is set and if the valid bit is set (set WB bit if valid bit V and dirty bit D are set; 8/6-59).

As to claim 38:

19) Middleton teaches wherein the predetermined amount of data is a line of cache data stored in a first level of a memory hierarchy and wherein the write back bit indicates that the cache data is pending a write back to a second level of the memory hierarchy and wherein the dirty bit indicates that the block of data has been modified while in the first level of the memory hierarchy (8/5-46).

Claim Rejections - 35 USC § 103

20) The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21) Claims 18,43,44,46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marshall, Jr. et al (US 6,134,634) "Marshall".

As to claim 18:

22) Marshall teaches a cache but does not specifically teach the cache being SRAM. It is well-known and common to use fast memory, such as SRAM, for cache memory because of its speed. Thus it would have been obvious to one of ordinary skills in the art to use SRAM for the cache of Marshall for its speed.

As to claim 43:

23) Marshall teaches a system comprising: a circuit for setting/storing a status corresponding to a block of data in response to a change in address mapping to indicate that the block of data is pending write back (during context/process switching; set writeback bit P to indicate pending writeback; 2/58-3/7;5/3-15;9/28-51;11/40-56). Marshall does not specifically teach having antenna coupled to the first processor. Since "the first processor" does not have antecedent basis, the Examiner will interpret this limitation as "the circuit", as claimed. Marshall teaches using communication ports for connecting modems, network interfaces, etc. (communication port 103; Fig. 1; 6/1-6). Thus this suggests to one of ordinary skills that Marshall's invention can communicate to other devices/systems. It is common to use a wireless network communication device (wireless network card) that uses an antenna to connect to wireless networks. Thus, it would have been obvious to one of ordinary skills to use a wireless network card connected to Marshall's communications ports to allow for wireless communications to other devices.

As to claim 44:

24) Marshall teaches preventing access to the data block until the writeback is completed (2/33-57).

As to claim 46:

25) Marshall does not specifically teach the system is a wireless phone. Applicant should note that renaming of the preamble from a "system" to a "wireless phone" does not give more patentable weight since no additional limitation is added to the body of the claim to signify the difference between a system and a wireless phone. The Examiner will treat the claimed invention of a system and a wireless phone to be the same since both have the same limitations, as disclosed and claimed in the body of the claim. Marshall teaches using communication ports for connecting modems, network interfaces, etc. (communication port 103; Fig. 1; 6/1-6). Thus this suggests to one of ordinary skills that Marshall's invention can communicate to other devices/systems. It is common to use a wireless network communication device (wireless network card or wireless modem) that uses an antenna to connect to wireless networks. Thus, it would have been obvious to one of ordinary skills to use a wireless phone connected to Marshall's communications ports to allow for wireless communications to other devices.

Allowable Subject Matter

26) Claims 6-8,11-16,24-27,34,37,42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

27) As to claim 6, the prior art does not further teach wherein the status is a bit in a cache tag field and wherein the cache tag field includes information associated with the block of data,

and wherein setting includes setting the bit in response to the change in address mapping to indicate that the block of data is pending write back from a first level of a memory hierarchy to a second level of the memory hierarchy and to indicate that the block of data in the first level of the memory hierarchy is not accessible with the current address mapping.

28) As to claim 7, the prior art does not further teach wherein the status is a bit in a cache tag field, wherein the cache tag field includes information associated with the block of data that is stored in a cache memory, and wherein setting the bit includes setting the bit if the block of data is valid and dirty.

29) Claim 8 is also allowable for incorporating the limitations of claim 7, and further limitations.

30) As to claim 11, the prior art does not further teach wherein the status is encoded in at least one bit in a cache tag.

31) Claims 12-16 are also allowable for incorporating the limitations of claim 11, and further limitations.

32) As to claim 24, the prior art does not further teach wherein the information is at least one bit in a cache tag.

33) Claims 25-27 are also allowable for incorporating the limitations of claim 24, and further limitations.

34) As to claim 34, the prior art does not further teach wherein the first level of the memory is a cache memory and further including storing the at least one bit in the cache memory.

35) As to claim 37, the prior art does not further teach comprising setting the write back bit in response to a change in address mapping in a virtually addressed system.

36) As to claim 42, the prior art does not further teach wherein the processor includes logic to translate virtual addresses to physical addresses, the first level of the memory hierarchy is a cache memory, the predetermined amount of data is a line of cache data, and the at least one bit is in a cache tag field associated with the line of cache data and the at least one bit is stored in the cache memory.

37) Claim 45 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

38) As to claim 45, the prior art does not further teach wherein the system includes a processor that includes the circuit, the processor includes logic to translate virtual addresses to physical addresses, the first level of the memory hierarchy is a cache memory, the predetermined amount of data is a line of cache data, and the at least one bit is in a cache tag field associated with the line of cache data and the at least one bit is stored in the cache memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Than Nguyen
Primary Examiner
Art Unit 2187